Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1. (Currently amended) A memory module comprising[[,]]:
 - a plurality of memory circuits;
 - a plurality of data lines coupled to the plurality of memory circuits, the plurality of data lines transfer data to and from the plurality of memory circuits;
 - a switching device coupled to at least one of the plurality of data lines, the switching device attached to the outer surface of one of the plurality of memory circuits; and
 - wherein the switching device selectively operates to simulate a hardware error on at least one of the plurality of data lines based on an input signal from a control logic external to the memory module.
- 2. (Original) The memory module of claim 1 wherein the memory circuits are packaged memory circuits, and wherein the switching device is attached to an outer surface of the package of one of the plurality of memory circuits.
- 3. (Original) The memory module of claim 1 wherein the switching device electrically floats the at least one of the plurality of data lines.
- 4. (Original) The memory module of claim 1 wherein the switching device drives the at least one of the plurality of data lines to a high voltage level.
- 5. (Original) The memory module of claim 1 wherein the switching device drives the at least one of the plurality of data lines to a low voltage level.

- 6. (Original) A method comprising:
 - receiving a request by a control logic to simulate a hardware error on a data line of a memory module; and
 - simulating the hardware error on the data line by a switching unit on the memory module.
- 7. (Original) The method of claim 6 further comprising sending instructions to inject the error to the control logic from an application executing in a computer system coupled to the memory module.
- 8. (Original) The method of claim 7 comprising sending the instructions on a communication bus.
- 9. (Original) The method of claim 8 comprising sending the instructions on an inter-integrated circuits (I²C) communications bus.
- 10. (Original) The method of claim 6 wherein simulating the hardware error comprises driving a high voltage on the data line in the memory module to simulate a stuck-at-1 hardware error.
- 11. (Original) The method of claim 6 wherein simulating the hardware error comprises electrically floating a data line in the memory module to simulate a stuck-open hardware error.
- 12. (Original) The method of claim 6 wherein simulating the hardware error comprises electrically grounding the data line in the memory module to simulate a stuck-at-0 fault.
- 13. (Original) The method of claim 6 wherein simulating the hardware error comprises simulating a hardware error for a predetermined amount of time, the simulated hardware error being one selected from the group consisting of a stuck-

at-1 hardware error, a stuck-at-0 hardware error, and a stuck-open hardware error.

- 14. (Currently amended) A system comprising:
 - a central processing unit (CPU);
 - a memory coupled to the CPU; and
 - control logic coupled to the memory and to the CPU, the control logic operable by the CPU to enable operation of a switching device coupled to a memory module to simulate a hardware error in the memory module;
 - wherein the switching device and the memory module are both physically located inside the system.
- 15. (Original) The system of claim 14 wherein the switching device is operable to apply a high voltage level to a data line in the memory module.
- 16. (Original) The system of claim 14 wherein the switching device is operable to apply a low voltage level to a data line in the memory module.
- 17. (Original) The system of claim 14 wherein the switching device electrically floats a data line in the memory module.
- 18. (Original) The system of claim 14 wherein the control logic initializes and maintains a counter of the number of hardware errors to simulate in memory module.
- 19. (Original) The system of claim 14 wherein the control logic initializes and maintains a timer of the duration of hardware errors to simulate in the memory module.

- 20. (Currently amended) A system comprising:
 - a plurality of means for storing data, wherein at least one of the means for storing data is integrated with a means for driving a simulated hardware error;
 - a plurality of means for transferring data to and from the plurality of means for storing data; and
 - wherein the means for driving is operable to one of drive a voltage and electrically float at least one of the plurality of means for transferring data.
- 21. (Original) The system of claim 20 wherein the means for driving applies a voltage based on a request from a software application.
- 22. (Original) The system of claim 20 wherein the means for driving further comprises a means for interfacing with a communications bus.